

OPERATION MANUAL

MODEL S500S1024

DIGITAL CORRELATION SPECTROMETER

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1. SPECIFICATION

a. Clock Input

This input is AC coupled and accepts sine or square wave with an amplitude in the range of 0.5 to 1 V peak-to-peak. The frequency of the clock ranges from 1 MHz to 1 GHz. The return loss at this input is greater than 15 dB over the specified frequency range.

b. Signal Input

This input is AC coupled and accepts noise signals, received typically from the IF section of a radio-telescope, with a maximum analog bandwidth ranging from 1 MHz to 500 MHz. The power at this input should be from -3 dBm to +3 dBm for a 500 MHz bandwidth noise signal. If CW signals are used at this input, the amplitude should be in the range of 10 mV to 1V peak-to-peak. The return loss at this input is greater than 15 dB over the maximum frequency range. To avoid aliasing, always use a low-pass filter appropriate for the selected clock frequency.

c. Parallel Port

The parallel port of the S500S1024 digital correlation spectrometer should be connected to the EPP parallel port LPT2 (at address 278H) of a personal computer running the Windows 95 operate system.

d. Frequency Resolution

The S500S128 calculates and displays 1024 frequency channels of the power spectrum of band limited input signal. The frequency resolution is calculated as the signal bandwidth divided by the 1024 frequency channels. At the maximum signal bandwidth of 500 MHz the frequency resolution is 0.5 MHz. Frequency resolution can be increased by decreasing the clock frequency and thus the bandwidth.

e. Integration Time

The integration time can be set from 100 ms to 22 seconds at the maximum clock frequency of 500 MHz. The maximum integration time increases proportionally with the decrease in clock frequency because the integration counter is synchronized with submultiple signal derived from the digitizer clock.

f. Dimensions and Weight

The S500S1024 digital correlation spectrometer is enclosed in a 19 inch rack mountable box with a height of 7 inches and a depth of 24 inches. (H=177mm, W=426mm, D=610mm). Net weight is approximately 48 lb (48 Kg).

g. Power Requirements

110-120 V , 47-63 Hz, 300 VA

h. Temperature

Operating range: From 0 degree C to 45 degrees C. The S500S1024 Correlation Spectrometer is provided with three cooling fans at the front panel and two cooling fans at the back panel. Maintain a clearance of about 10 inches to ensure adequate air flow, otherwise the temperature in the enclosure will exceed the specified requirements. The instrument is protected with a temperature cut-off switch which is thermally activated at 25 degrees C and will disconnect the AC power from the instrument.

Storage range: From -40 degrees C to 75 degrees C.

i. Humidity

Maximum humidity : 95%RH at 40 degrees C.

2. THEORY OF OPERATION

Digital correlation spectrometers are used for measuring an estimate of the power spectral density of signals corrupted by noise. In most practical applications, the noise is approximated as a Gaussian random process with zero averages and the signals are assumed ergodic, independent, and small relative to the noise. When the combination of Gaussian noise with this type of signals has an extremely small signal-to-noise ratio, it is often referred to as partially coherent noise signals, or noise-like signals, or simply noise signals.

The estimate of the power spectral density of a band-limited noise signal could be generated in real-time with the S500S1024 digital correlation spectrometer which comprises a digitizer, eight digital correlator chips (seven S500C128 and one S500c128A), and a parallel port interface to a personal computer system (Fig. 1). The digitizer is a special type of analog-to-digital converter which quantizes and samples the noise signal. The correlator digital chip, a special-purpose integrated circuits, calculates the correlation function of the noise signals. Finally, the general-purpose computer system performs a correction of the correlation function to remove some of the quantization errors introduced by the digitizer, calculates a fast Fourier transform of the corrected correlation function and displays an estimate of the power spectral density.

The digitizer used in the S500S1024 digital correlation spectrometer resembles a conventional analog-to-digital converters in that both perform quantization and sampling. However, they are different in the way decision levels and weights are assigned to the quantizers. Additionally, the digitizer is relatively simple since sufficiently accurate estimates of the power spectra could be obtained with the S500S1024 correlation spectrometer even when noise signals are coarsely quantized on four levels -- each sample being represented by only 2 bits.

For a band-limited noise signal quantized on four levels and sampled at the Nyquist frequency, the digital representation has a lower signal-to-noise ratio than the original analog noise signal by a factor of 0.87. This factor (sometimes expressed in percentages) by which the signal-to-noise ratio of a digitized signal decreases, relative to the analog noise signal, is also known as the efficiency of the digitizer. It is also customary that instead of characterizing digitizers in terms of their efficiency, the inverse of this is used and called sensitivity degradation factor. The sensitivity of the 2-bit digitizer with 4 quantization levels sampled at the Nyquist frequency is 1.14 when the decision levels of the quantizers are optimized and weighting factors are assigned to each quantization levels.

The transfer characteristic of the digitizer is illustrated in Fig. 2. The normalized rms voltage of the analog noise signal is plotted on the abscissa while the 2-bit encoded digital output states and the weights are shown on the ordinate. The analog noise signal is divided in four quantization levels by three threshold voltages V_L , V_0 , and V_H which are chosen to be -0.9, 0, and +0.9 times the rms voltage of Gaussian noise, respectively. The most significant bit of the digital output word represents the sign and the least significant bit represents the magnitude of the digitized analog noise signal. If the voltage of the analog noise signal is positive then the sign bit is assigned the logic value 0 or 1 if it is negative. The magnitude bit is assigned the logic value 0 if the voltage of the analog noise signal is between V_L and V_H and it is assigned the logic value 1 if it is outside those two threshold voltages. Additionally, weighting factors -3, -1, +1, and +3 are assigned to the four digital output states 01, 00, 10, and 11, respectively. The choice of the value of these weights gives a uniform step of two units from one digital state to any adjacent one.

Maintaining correct threshold levels in the digitizer in terms of the rms voltage of the Gaussian noise input is much more difficult than another procedure that is based on the counts of the relative frequency of occurrence of different digital states. To implement a threshold adjustment procedure based on the frequency of occurrence it is necessary to connect to the digitizer output four frequency counters C01, C00, C10, and C11, for counting the number of samples that occur in each digital state 01, 00, 10, and 11, respectively.

Correct setting of threshold voltages is performed with Gaussian noise applied at the analog input of the digitizer. The correct threshold voltage for V_0 is attained when the contents of $C_{01}+C_{00}$ and that of $C_{10}+C_{11}$ are equal, because the total number of samples with the negative sign bit equals the total number of samples with the positive sign bit. The digitizer is optimized when the threshold voltage V_h operates at 0.9 times the rms voltage of Gaussian noise input which corresponds to setting V_h such that 36.8% of the samples with the positive sign bit ($C_{10}+C_{11}$) are in counter C_{11} - Similarly, V_l should be adjusted so that 36.8% of the samples with the negative sign ($C_{01}+C_{00}$) are in counter C_{01} . A simplified schematic diagram of the 2-bit, 4-level digitizer with the capability of setting threshold voltages based on the contents of four frequency counters located on the first S500C128 chip is depicted in Fig. 3.

The S500C128 and the S500C128A are special-purpose custom CMOS integrated circuits, implemented as a 2x2 array of correlator cells (Fig. 4), which calculates an estimate of the correlation function between a set of digitized data inputs X and another set of digitized data inputs Y. Each set of data inputs X and Y comprises an even (E) data input and an odd (O) data input. Furthermore, each even and odd data input is encoded on two bits -- one representing a sign (S) bit and the other a magnitude (M) bit.

For reliable operation, all digitized data inputs are differential (dual-rail) with one true rail and another complementary rail labeled as bar (B). For each digitized data input, there is a corresponding data output with a label terminating in 0 rather than in 1. The same input data appears at a corresponding output after a fixed number of clock cycles. For example, the X, even (E), magnitude (M), differential data input is labeled as (XEMI,XEMBI) and its corresponding differential data output is labeled (XEMO,XEMBO).

The S500C128 chip calculates a 128-point estimate of the correlation function between the X and Y signals sampled at a maximum data rate of 1 Gs/s and digitized in four quantization levels with weighting factors of -3, -1, +1, and +3. Consequently, the correlator chip can analyze signals with a maximum frequency of 500 MHz and has 87% of the signal-to-noise ratio of a continuous correlator. The 500 MHz bandwidth is accomplished with a clock frequency of 500 MHz (not 1 GHz) because the 2x2 array of correlator cell processes data in parallel with a time multiplexing factor of 2.

A correlator cell calculates the cross-correlation function of a prompt input signal (P_{IN}) and a delayed input signal (D_{IN}). The D_{IN} signal is generated with a tapped shift register while the P_{IN} signal is broadcast undelayed, relative to D_{IN} to all lags. Each lag computes correlation products from the P_{IN} and D_{IN} signals and subsequently accumulates these products in a counter.

The correlator cell comprise four shift registers for the digitized data. Two of the shift registers are for the P_{IN} and two more shift registers are for the D_{IN} . One of the two shift registers is for the sign bit and the other one is for the magnitude bit. A simplified block diagram of a correlator cell showing only one of the shift register for the P_{IN} and another one for the D_{IN} appears in Fig. 5. The shift register for the P_{IN} has an output tap after each flip-flop while the taps of the D_{IN} shift register are located after every two flip-flops. Each lag is made of a 2x2 bit multiplier, a 3bit accumulator, a 32-bit counter, and four 32-bit buffer/shift registers. The contents of the accumulator can not be read out from a correlator chip. Only the contents of the four buffer/shift registers can be read out by a computer.

The logic diagram of one of the 2x2-bit pipelined multiplier-accumulators is shown in Fig. 6. The overflow of the multiplier-accumulator is integrated by a 32-bit counter. The 32-bit counter is implemented with conventional toggle flip-flops made from static CMOS gates. In order to allow the carry to propagate through the counter, before transferring the data to the buffer register, a synchronized gate circuit is used to isolate the counter from the accumulator. The 32-bit buffer register is designed to receive data in parallel from the counter. In one mode of operation the buffer register receives 32-bits of data from the counter and in another mode the data from the

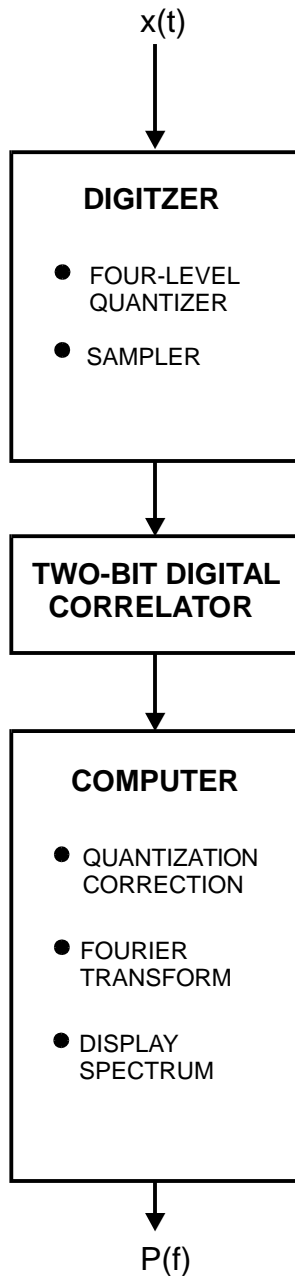
buffer are shifted out from the chip by a host computer. The synchronized gate circuit is used to interrupt the connection between the prescaler and the counter without chopping the signal.

The procedure for reading out the contents of the counters is as follows. First, the inputs of all the counters are disconnected from the outputs of the accumulator by an control signal labeled GCI (Gate Counter Input). (Note that the names of the control signals that appear in *italics* indicate that the corresponding inputs and outputs are electrically compatible with TTL levels.) Second, the correlation coefficients accumulated in the counters are transferred to one of the 32bit shift registers by asserting control signal TCI (Transfer Counter Input). Third, all the counters are set to zero by control signal CLRI (Clear Input). Fourth, the GCI control signal is activated to reconnect the inputs of the counters to the outputs of their corresponding accumulator, so that a new calculation of correlation coefficients can be made. Finally, the correlation coefficients residing now in one of the shift registers are shifted out through the SDO (Shift Data Out) port, one bit a time in synchronism with the SCI (Shift Clock Input). The SDI (Shift Data Input) is provided for testing the shift register, The read out starts with the highest numbered lag (lag 127) and continues in descending order of lags. Additionally, the bits of odd lags are shifted out in descending order and those of even lags in ascending order.

A correlator cell comprises 64-lags which operate at a clock frequency of 500 MHz with a bandwidth of 250 MHz. The longest integration time is determined by the 32-bit counter. At a clock frequency of 500 MHz, the correlator chip can accumulate, without overflowing, for approximated 34 seconds. The shortest integration time is determined by the interval of time required to read out the contents of the buffer/shift registers.

The idle time (blanking) of the correlator is reduced substantially by attaching four buffer registers to each counter (quadruple buffering is a desirable feature which reduces blanking time in interferometry with both phase and Dicke switching). This way, only one clock cycle is required to transfer all 32 bits of the counters to the attached buffer registers. After the transfer, all the counters are cleared and the computation of correlation continues. The contents of the buffer registers are read out concurrently with a computational of new correlation coefficients. It is estimated that the blanking time (the time to transfer the contents of the counters to the buffers) of the proposed correlator will not exceed 10 nsec. The short blanking time is useful in the observation of short events such as solar flares. Each correlator will be provide with a 32-bit bus. Thus, the contents of two buffers, one from each correlator, will be read out simultaneously at a read-clock frequency of 60 MHz. The total read-out time per chip is estimated at less than 100 msec.

The architecture of the correlator permits cascading of several chips to form a digital correlating spectrometer with more than 256 channels since the X and Y signals are provided as outputs from two internal shift registers.



Restriction on the input signal, $x(t)$:

- 1) Must be a gaussian random signal
- 2) Must have a band-limited power spectrum,
 $P(f) = 0$ for $f > Bw$

Quantizing operation as shown in Fig. 2

Sampling frequency, $F_s = 2Bw$

Each sample is a two-bit digital number every

T_s seconds, $T_s = \frac{1}{F_s}$

Calculates a two-bit, four level correlation function.

Correlation takes place for T seconds.

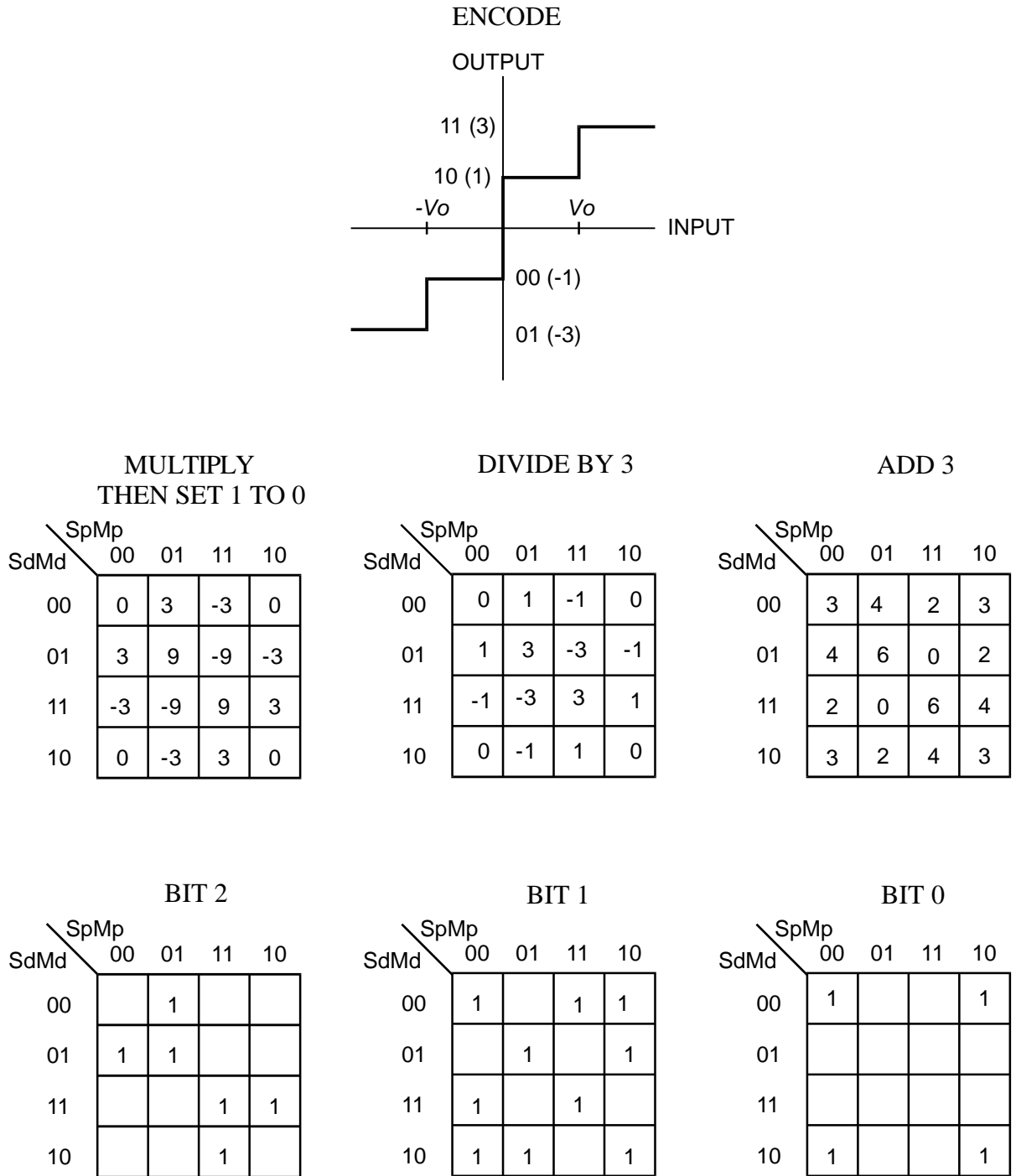
The correlation functions is read out of the correlator and is fed into a computer.

The errors caused by quantization are corrected.

The spectral estimate is computed as a Fourier transform of the correlation function.

The spectrum is displayed.

Fig. 1 Block diagram of a digital correlation spectrometer



$$\text{BIT 0} = \overline{\text{Md} + \text{Mp}}$$

$$\text{BIT 1} = \text{BIT 0} + \text{Md.Mp} \oplus (\text{Sd} \oplus \text{Sp})$$

$$\text{BIT 2} = \overline{\text{BIT 0} + \text{Sd} \oplus \text{Sp}}$$

Fig. 2 The transfer function of an optimized 2-bit 4-level digitizer

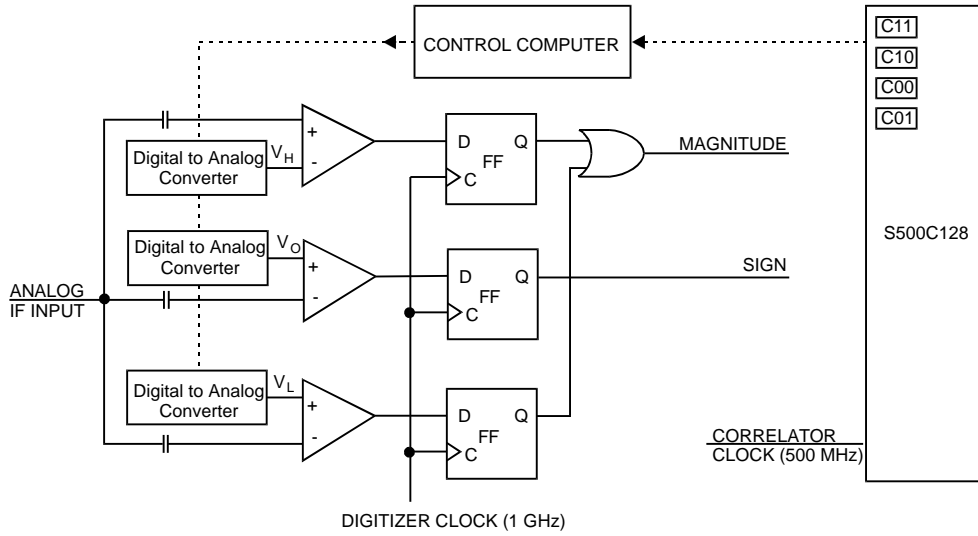


Fig. 3 A digitizer with the capability of setting threshold voltages based on the contents of four frequency counters

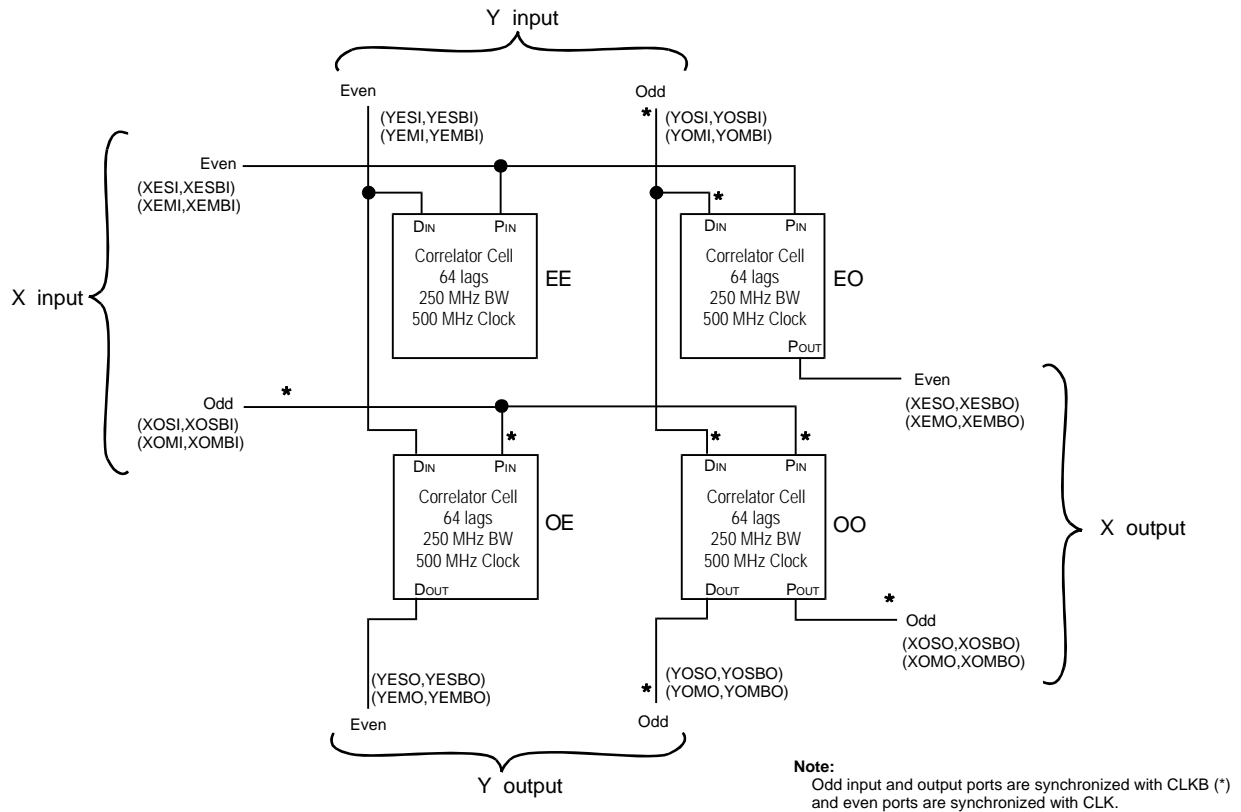


Fig. 4 The parallel processing architecture of the 128-lag correlator comprises a 2x2 array of correlator cells and uses a time multiplexing factor of 2 to achieve a bandwidth of 500 MHz at a clock frequency of 500 MHz

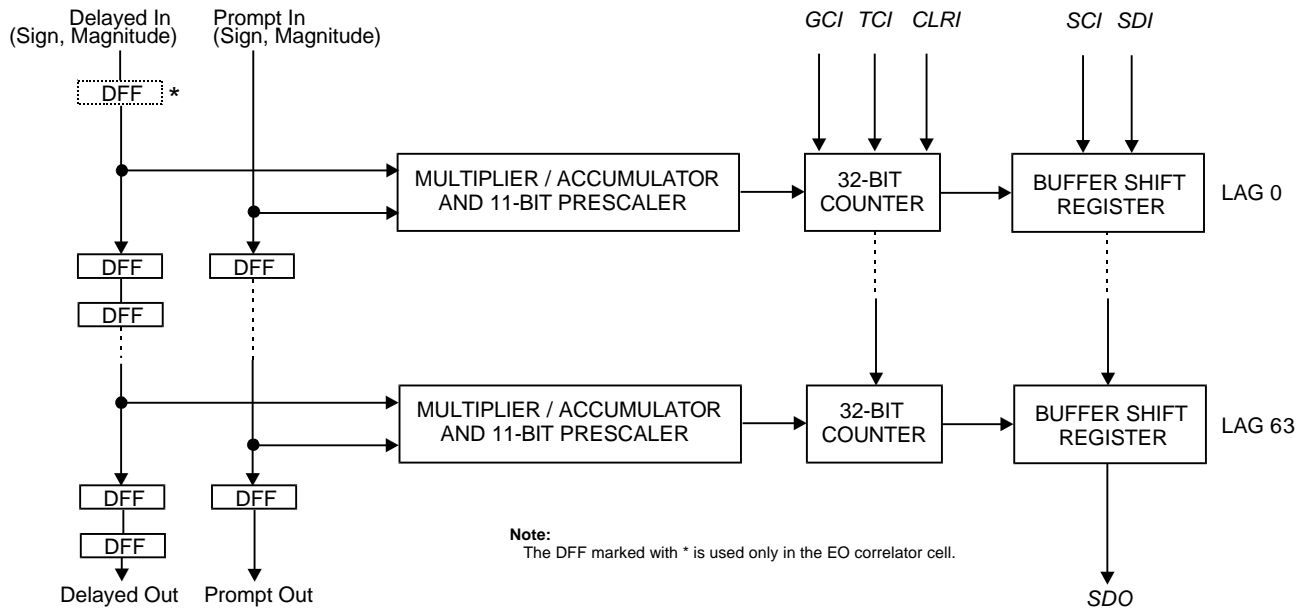


Fig. 5 A simplified diagram of a correlator cell with 64 lags, 250 MHz bandwidth, and 500 MHz clock.

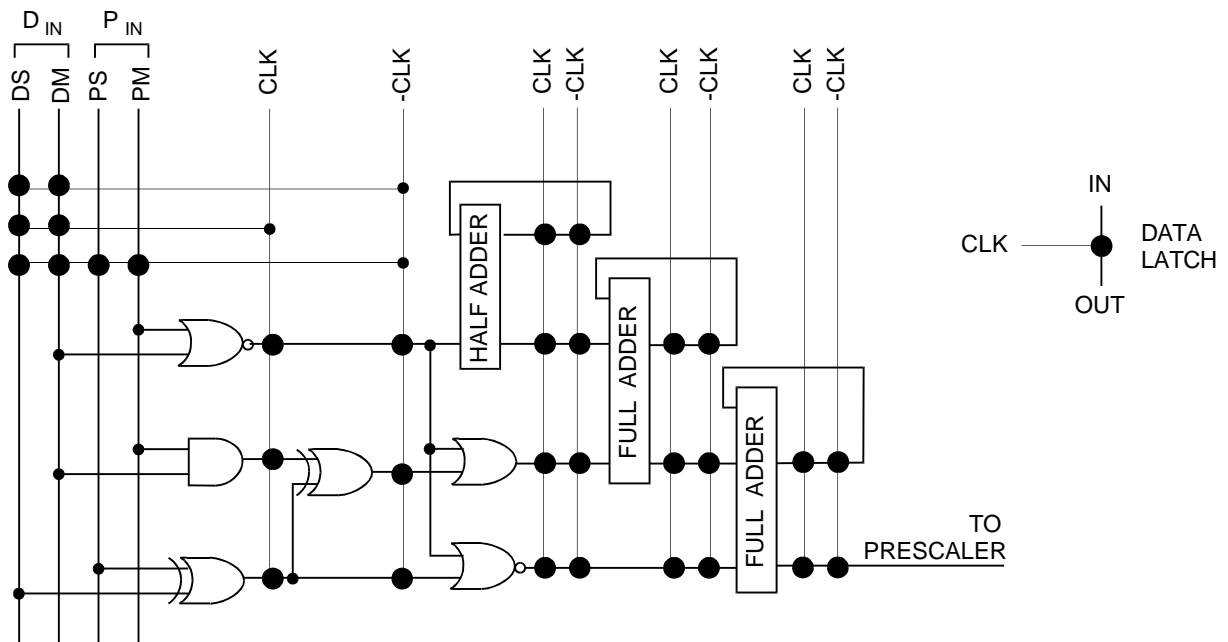


Fig. 6 The pipelined modified 2x2-bit multiplier-accumulator

3. PROGRAMMING NOTES

a. Correlation Spectrometer System

The auto-correlation spectrometer comprises a 2-bit digitizer, two programmable chip, nine delay lines, a temperature sensor, and eight chips (seven S500C128 and one S500C120A). The 2-bit digitizer has three digital to analog converters for threshold voltage adjustment. The chips contains a PC interface circuit, and an integration timer. The delay lines are Motorola MC100E195. The chip is a 128-channel, 2-bit, 4-level correlator.

The three digital to analog converters used on the digital correlation spectrometer board are Analog Devices AD1861. They have the following features: 18-bit, 2's complement, serial input. (See section h for adjustment procedure.)

The integration timer is implemented in the . chips The integration timer is a 16-bit count-down counter. The clock to the integration timer is derived from the system clock through a 25-bit prescaler, i.e., the clock to the integration timer equal the system clock divide by 2 to the power 25. (See section f for setting procedure.)

A Motorola (MC100E195) 128-step programmable delay line is used to provide the delay between the clock and the data input of the chips. This delay line has 20 ps digital step resolution. (See section i for setting procedure.)

A National Semiconductor temperature sensor (LM35DM) is placed near the on the heat sink to monitor the temperature. This sensor is used in combination with a Linear Technology A/D converter (LTC1286).

b. Enhanced Parallel Port

The digital correlation spectrometer communicates with a PC through an Enhanced Parallel Port (EPP). The EPP has the following features:

<u>Port Name</u>	<u>Offset</u>	<u>Mode</u>	<u>R/W</u>	<u>Description</u>
SPP Data	+0	SPP/EPP	W	Standard Parallel Port data. No autostrobing.
SPP Status	+1	SPP/EPP	R	Reads the input status lines on the interface.
SPP Control	+2	SPP/EPP	W	Sets the state of the output control lines.
EPP Address	+3	EPP	R/W	Generates an interlocked address read or write cycle.
EPP Data	+4	EPP	R/W	Generates an interlocked data read or write cycle.
Not Defined	+5,6,7	EPP	N/A	May be used for 16 and 32 bit I/O.

<u>Pin</u>	<u>Signal Name</u>	<u>In/Out</u>	<u>Description</u>
1	nWRITE	Out	Active low. Low indicates a write cycle. High for a read cycle.
2-9	A/D[0:7]	Bi	Bi-directional address/data lines.
10	nINTR	In	Peripheral interrupt. Used to generate an interrupt to the host.
11	nWAIT	In	Handshake signal. Low: OK to start a cycle. High: OK to end a cycle.
12	User defined	In	Can be used differently by each peripheral.
13	User defined	In	Can be used differently by each peripheral.
14	nDATASTB	Out	Active low. Indicates a Data Read/Write cycle is in process.
15	User defined	In	Can be used differently by each peripheral.
16	nRESET	Out	Active low. Peripheral reset.

17 nADDRSTB Out Active low. Indicates an Address Read/Write cycle is in process.
 18-25 GND

c. Address Space of the Correlation Spectrometer

The addresses of the correlation spectrometer are distributed as follow:

Address for WRITE	Usage
00h - 03h	write four bytes of the integration timer.
04h	load the integration timer and let it counts down.
05h	set shift data for a threshold voltage D/A.
06h	set shift clock for a threshold voltage D/A.
07h	chip select of D/A of VT0.
08h	chip select of D/A of VTL.
09h	chip select of D/A of VTH.
10h	send a latch enable to the first delay line (board).
11h	send a latch enable to the second delay line (chip 1).
12h	send a latch enable to the third delay line (chip 2).
13h	send a latch enable to the fourth delay line (chip 3).
14h	send a latch enable to the fifth delay line (chip 4).
15h	send a latch enable to the sixth delay line (chip 5).
16h	send a latch enable to the seventh delay line (chip 6).
17h	send a latch enable to the eighth delay line (chip 7).
18h	send a latch enable to the ninth delay line (chip 8).
19h	send delay value into the Xilinx buffer register.
1Ah	latch five controlling bits into the Xilinx buffer register.
1Bh	set the control mode (0=auto, 1>manual).
1Ch	set the swap mode (0=no swap, 1=swap bit ordered).

Address for READ	Usage
10h	read a formatted byte from the first correlator chip.
11h	read a formatted byte from the second correlator chip.
12h	read a formatted byte from the third correlator chip.
13h	read a formatted byte from the forth correlator chip.
14h	read a formatted byte from the fifth correlator chip.
15h	read a formatted byte from the sixth correlator chip.
16h	read a formatted byte from the seventh correlator chip.
17h	read a formatted byte from the eight correlator chip.

d. Programming the Xilinx Chips

- After power on wait until bit 5 at base+1 goes high.
- Send data one bit at a time to bit 0 (for Xilinx on digitizer board) and to bit 1 (for Xilinx on correlator board) at address base+4 (EPP data port).

Repeat step b until all configuration bits are sent.

- The Xilinx is ready when bit 4 at base+1 goes high.

e. Setting the Integration Timer

Write the integration timer

- a. Send 00h to base+3 (EPP address port).
- b. Send byte 0 to base+4 (EPP data port).
- c. Send 01h to base+3 (EPP address port).
- d. Send byte 1 to base+4 (EPP data port).
- e. Send 02h to base+3 (EPP address port).
- f. Send byte 2 to base+4 (EPP data port).
- g. Send 03h to base+3 (EPP address port).
- h. Send byte 3 to base+4 (EPP data port).

Set control mode to auto

- i. Send 1Bh to base+3 (EPP address port).
- j. Send 01h to base+4 (EPP data port).

Load and start the integration timer

- i. Send 04h to base+3 (EPP address port).
- j. Send 01h to base+4 (EPP data port).

f. Adjusting the Threshold Voltage

Send 18-bit control data to the D/As serially, MSB first. Each bit is sent as follow:

- a. Send 05h to base+3 (EPP address port).
- b. Send one bit from control data to base+4 (EPP data port).
- c. Send 06h to base+3 (EPP address port).
- d. Send 01h (shift clock high) to base+4 (EPP data port).
- e. Send 00h (shift clock low) to base+4 (EPP data port).

Select which threshold voltage D/A

- a. Send 07h (07h for VT0, 08h for VTL, 09h for VTH) to base+3 (EPP address port).
- b. Send 01h to base+4 (EPP data port).
- c. Send 00h to base+4 (EPP data port).

g. Adjusting the Clock Delay

On the correlator board, there are a clock delay line for the board and for each correlator chip. The delay line can be adjusted in 128 steps (7 bits), each with 17 ps. To adjust a delay line, first send the delay value to the board, then send a latch enable to the delay line to be adjusted.

- a. Send 19h to base+3 (EPP address port).
- b. Send delay value to base+4 (EPP data port).
- c. Send latch enable signal (10h to 18h) to base+3 (EPP address port).

h. Reading the Correlator Counters

The content of each correlator chip are shifted out serially into the Xilinx. Inside the Xilinx, every 8 bits are converted to a byte. For a fully populated board, 8 serial shifted streams are done at the same time. For each correlator chip, the read out starts with the highest numbered lag (lag 127) and continues in descending order of lags, then counter 01, counter 00, counter 10, and counter 11. Additionally, the bits of odd lags, counter 01, and counter 10 are shifted out in descending order and those of even lags, counter 00, and counter 11 in ascending order. Thus, it is necessary to swap the bit when one reads the content of the even lags, counter 00, and counter 11.

The content of the correlator can be read out at a precise interval by using the integration timer in the Xilinx on the digitizer board. The following sequence is used to read the content of the correlator.

Polling to check for the terminate signal (active low) of the integration timer:

- a. Read base+1 and check bit 0.

Switch the control mode (address 1B) from 1 (auto) to 0 (manual):

- b. Send 1Bh to base+3 (EPP address port).
- c. Send 00h to base+4 (EPP data port).

Set the swap mode to no swap

- d. Send 1Ch to base+3 (EPP address port).
- e. Send 00h to base+4 (EPP data port).

Provide eight shift clocks. Do g and h eight times

- f. Send 1Ah to base+3 (EPP address port).
- g. Send 01h to base+4 (EPP data port).
- h. Send 00h to base+4 (EPP data port).

Read one byte from each correlator chip.

- i. Send 10h to base+3 (EPP address port).
- j. Read the first correlator from base+4 (EPP data port).
- k. Send 11h to base+3 (EPP address port).
- l. Read the second correlator from base+4 (EPP data port).
- m. Send 12h to base+3 (EPP address port).
- n. Read the third correlator from base+4 (EPP data port).
- o. Send 13h to base+3 (EPP address port).
- p. Read the forth correlator from base+4 (EPP data port).
- q. Send 14h to base+3 (EPP address port).
- r. Read the fifth correlator from base+4 (EPP data port).
- s. Send 15h to base+3 (EPP address port).
- t. Read the sixth correlator from base+4 (EPP data port).
- u. Send 16h to base+3 (EPP address port).
- v. Read the seventh correlator from base+4 (EPP data port).
- w. Send 17h to base+3 (EPP address port).
- x. Read the eighth correlator from base+4 (EPP data port).

Repeat from steps f through x three more times to read all 32 bits of the counter of a lag. Next, change the swap mode to swap (1) and repeat from steps f through x four times to read the counter of the

next lag. The process is continue until all the counters are read out. Note that each correlator chip have 128 lags and four test counters. Thus, the total of counter to be read out is 132.

i. Setting the DIP Switches

There are four dip switches on the digitizer board. These dip switches are used to provide feed back for EPP hand shaking signal.

If the digitizer board was used alone, set

switch 2	off
switch 3	on
switch 4	on

If the digitizer board was used with the correlator board (default setting) , set

switch 2	on
switch 3	off
switch 4	off

4. APPENDIX

S500C128 SPECIFICATION

S500C128A SPECIFICATION